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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/911,581	07/25/2001	Takahiro Ohnakado	401308	6065

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EXAMINER	
RICHARDS, N DREW	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 01/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/911,581	OHNAKADO, TAKAHIRO	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *9-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 12* is/are rejected.

7)☒ Claim(s) *7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-8 in Paper No. 7 is acknowledged.

Specification

2. 35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are: Page 2 lines 1-2 "the phenomenon happened at semiconductor device", Page 2 line 22 "these destruction".

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. (U.S. Patent No. 5939753) in view of Wang (U.S. Patent NO. 6351363 B1).

Ma et al. disclose in figures 8 and 10, a substrate 11, a Si MOS transistor 115 and an ESD protection circuit 160 in high frequency devices. Ma et al. do not disclose the ESD circuit having a first lateral polysilicon diode on the substrate, the first lateral polysilicon diode having a forward direction and a reverse direction, wherein the first lateral polysilicon diode connects, in the forward direction, a high-frequency I/O signal line to an externally supplied voltage.

Wang teaches an ESD circuit. Wang teaches in figure 3, an ESD circuit comprising a first lateral polysilicon diode 11 on a substrate, the diode having a forward direction and a reverse direction, wherein the diode connects, in the forward direction, a I/O signal line to an externally supplied voltage VDD. In combination, the diode of Wang would connect to a high-frequency I/O signal line of Ma et al.

With regard to claim 2, Ma et al. does not teach a second lateral polysilicon diode. Wang teaches a second polysilicon diode 12 in figure 3, the diode having a forward direction and a reverse direction and is connected in the forward direction between ground (VSS in figure 3, disclosed as ground on column 4 line 6) and an I/O signal line, which in combination would be a high-frequency signal line of Ma et al.

Ma et al. and Wang are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form a first and second lateral polysilicon diode connected between the I/O signal line and Vdd and the signal line and ground, respectively, as the ESD protection circuit. The motivation for doing so is the use of lateral polysilicon diode provides faster ESD protection response as it is isolated from the substrate and has no

parasistic substrate capacitance. Therefore, it would have been obvious to combine Ma et al. with Wang to obtain the invention of claims 1 and 2.

With regard to claim 3, the ESD circuit comprises m diodes connected between I/O and VDD and n diodes connected between ground and I/O, where m=1 and n=1. Applying a specified voltage is merely an intended use that does not structurally distinguish over the prior art. It is obvious to one of ordinary skill in the art that a voltage VDD of 2 Volts could be applied to the device.

With regard to claim 4, in the combination of Ma et al. with Wu, no lateral polysilicon diode is connected to any signal line other than the high frequency I/O signal line as all the devices of Ma et al., and thus all signal lines, are considered high frequency devices.

With regard to claims 5 and 6, Ma et al. teach a capacitor having polysilicon upper and lower electrodes and a transistor having a polysilicon gate. Combined with Wang, which teaches a polysilicon diode, the diode and lower electrode of the capacitor are from a first polysilicon layer and the upper electrode of the capacitor and the gate are from a second polysilicon layer. Whether formed simultaneously or in different steps, the limitations of claims 5 and 6 only structurally limit the device to having the electrodes, gate, and diode of polysilicon.

With regard to claim 12, the ESD circuit of Wang further comprises a clamp circuit 130 connected between the externally supplied voltage VDd and ground (VSS in figure 3), wherein the clamp circuit permits current flow at a voltage lower than a reverse bias breakdown voltage of the first diode.

Allowable Subject Matter

5. Claims 7 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: Prior art of record fails to teach, disclose,or suggest, either alone or in combination, a Si MOS transistor, a lateral polysilicon diode connected between a high-frequency I/O signal line and VDD, and a capacitor having upper and lower polysilicon electrodes where the polysilicon of the upper electrode of the capacitor covers a PN junction of the first lateral polysilicon diode or where the capacitor includes a dielectric layer that covers the PN junction of the first lateral polysilicon diode.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Opris et al. ((U.S. Patent NO. 5973897), Horvath (U.S. patent NO. 6002569), Dabral et al. (U.S. Patent No. 6278312 B1), Williams (U.S. Patent NO. 6060752).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (703) 306-5946. The examiner can normally be reached on M-F 8:00-5:30; Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

NDR
January 13, 2003